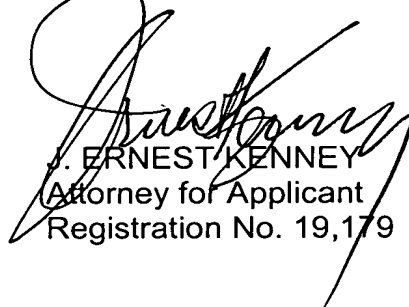


International Application No. PCT/EP00/03575
Attorney Docket: GRAS3003/JEK

REMARKS

Examination of the application as amended is respectfully requested.

Respectfully submitted,
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PATENT TRADEMARK OFFICE

09/926377

International Application No. PCT/EP00/03575
Attorney Docket: GRAS3003/JEK

APPENDIX OF CLAIMS

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1(Amended). A method for producing vertically integratable circuits, comprising producing electrically conductive contacts for vertical integration by simultaneously producing the integratable circuits themselves, electrically conductive contacts for vertical integration and electrically conductive contacts of the integrated circuit.

2(Amended). The method according to claim 1, comprising the steps:
a) producing an insulation at the places of the contacts for vertical integration from a front side of a substrate bearing the vertically integratable circuits,
b) producing a gap within the insulations from the front side,
c) filling the gaps with an electroconductive material from the front side,
d) exposing the electroconductive material from a backside of the substrate bearing the vertically integratable circuits at the places of the contacts for vertical integration, and
e) applying an electroconductive material from the backside to the previously exposed electric material at the places of the contacts for vertical integration.

3(Amended). The method according to claim 2, including thinning the substrate from the backside before exposure of the electroconductive material from the backside.

4(Amended). The method according to claim 3, wherein the substrate has a hidden insulating layer and thinning is performed up to said insulating layer.

5(Amended). The method according to claim 3, wherein thinning is performed until the insulation produced for the contacts for vertical integration is reached.

6(Amended). The method according to claim 2, wherein the insulation produced in method step a) is produced during production of field oxide, including forming gaps

in the substrate that enclose substrate material that oxidizes completely during production of the field oxide.

7(Amended). The method according to claim 2, wherein the gaps produced in method step b) within the insulations and the filling of said gaps according to method step c) with an electroconductive material are performed during production of a metalization level with associated through holes.

9/ 8(Amended). The method according to claim 2, including applying the electroconductive material applied in method step e) in a backside metalization.

9(Amended). A vertically integratable circuit having electrically conductive contacts for electrically conductive connection with further vertically integratable circuits, comprising electrically conductive contacts used for vertical integration and associated insulations produced simultaneously during production of the vertically integratable circuit itself.

10(Amended). The vertically integratable circuit according to claim 9, wherein at least two vertically integratable circuits are connected, and include electrically conductive contacts for vertical integration that are electrically connected with each other.



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PATENT TRADEMARK OFFICE

International Application No. PCT/EP00/03575
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APPENDIX OF MARKED UP VERSION OF CLAIMS

1(Amended). A method for producing vertically integratable circuits, [characterized in that] comprising producing electrically conductive contacts [(15)] for vertical integration [are produced using method steps serving to produce] by simultaneously producing the integratable circuits themselves, [the] electrically conductive contacts [(15)] for vertical integration and [the] electrically conductive contacts [(16)] of the integrated circuit [itself being produced simultaneously].

2(Amended). [A] The method according to claim 1, comprising the steps:

a) producing an insulation [(7, 8)] at the places of the contacts for vertical integration from [the] a front side of a substrate [(1, 2, 3)] bearing the vertically integratable circuits,

b) producing a gap [(13)] within the insulations [(7, 8)] from the front side,

c) filling the gaps [(13)] with an electroconductive material [(15)] from the front side,

d) exposing the electroconductive material [(15)] from [the] a backside of the substrate bearing the vertically integratable circuits at the places [(17)] of the contacts for vertical integration, and

e) applying an electroconductive material [(18)] from the backside[, in particular] to the previously exposed electric material [(15)] at the places [(17)] of the contacts for vertical integration.

3(Amended). [A] The method according to claim 2, [characterized in that] including thinning the substrate [is thinned] from the backside before exposure of the electroconductive material [(15)] from the backside.

4(Amended). [A] The method according to claim 3, [characterized in that] wherein the substrate [(1, 2, 3)] has a hidden insulating layer [(3)] and thinning is performed [as far as] up to said insulating layer [(3)].

5(Amended). [A] The method according to claim 3, [characterized in that] wherein thinning is performed until the insulation [(8)] produced for the contacts [(15)] for vertical integration is reached.

6(Amended). [A] The method according to [any of claims 2 to 5, characterized in that] claim 2, wherein the insulation [(8)] produced in method step a) is produced during production of field oxide, including forming [with] gaps [(4) being formed] in the substrate [(1)] that enclose substrate material [(5)] that oxidizes completely during production of the field oxide.

7(Amended). [A] The method according to [any of claims 2 to 6, characterized in that] claim 2, wherein the gaps [(13)] produced in method step b) within the insulations [(7, 8)] and the filling of said gaps according to method step c) with an electroconductive material [(15)] are performed during production of a metalization level [(16)] with associated through holes.

8(Amended). [A] The method according to [any of claims 2 to 7, characterized in that] claim 2, including applying the electroconductive material [(18)] applied in method step e) [is applied] in a backside metalization.

9(Amended). A vertically integratable circuit having electrically conductive contacts for electrically conductive connection with further vertically integratable circuits, [characterized in that the] comprising electrically conductive contacts [(15)] used for vertical integration and associated insulations [(7, 8) are] produced simultaneously during production of the vertically integratable circuit itself [simultaneously therewith].

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10(Amended). [A] The vertically integratable circuit according to claim 9, [characterized in that] wherein at least two vertically integratable circuits are connected, and [their] include electrically conductive contacts [(15, 18)] for vertical integration that are electrically connected with each other.

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